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B. E. (Third Semester) Examination, April-May 2020

(New Scheme)

(IT Branch)

DIGITAL ELECTRONICS and LOGIC DESIGN

Time Allowed: Three hours

Maximum Marks: 80

Minimum Pass Marks: 28

Note: Part (a) from each question is compulsory carrying 2 marks. Attempt any two parts from (b), (c) and (d) of each question carrying 7 marks each.

Unit-I

- 1. (a) Convert (1001011)₂ to decimal.
 - (b) Simplify the following Boolean function by using Tabulation method:

- (c) Simplify the following using K-Map:
 - (i) $F(W, X, Y, Z) = \Sigma m(2, 3, 12, 13, 14, 15)$
 - (ii) $F(A,B,C,D) = \Pi m, (1,4,5,11,12,14) \cdot d(6,7,15)$
- (d) Minimize and Implement the following multiple output functions:

$$f_1 = \sum m(1,2,3,6,8,12,14,15)$$

$$f_2 = \Pi m(0, 4, 9, 10, 11, 14, 15)$$

Unit-II

- 2. (a) What is Fan-in and Fan-out.
 - (b) With the help of a neat diagram, explain working of a two Input TTL NAND gate.
 - (c) Explain CMOS Invertor with its diagram & characteristic.
 - (d) Explain working of two input I²L NOR gate with its diagram.

[3]

Unit-III

- 3. (a) Explain Half Adder with its diagram.
 - (b) Design a BCD-to-XS-3 code convertor and also draw its logic diagram.
 - (c) Implement the Boolean function using 8×1 multiplexer select lines are A, B and D, as S_2 , S_1 & S_0 respectively.

$$F(A, B, C, D) = \sum (0,1,3,4,8,9,15)$$

(d) Design a 3 bit odd parity generator and check the parity using 4 bit odd parity checker.

Unit-IV

- 4. (a) Explain sequential circuit with a block diagram.
 - (b) Explain with diagram a 4 bit bidirectional shift Register.
 - (c) Design a synchronous counter using T Flip-flop that goes through states, 0, 3, 5, 6, 0 Is the counter self starting.
 - (d) Design a 4 bit Ring Counter using D flip-flops.

[4]

Unit-V

- 5. (a) Compare Moore Machine & Meelay Machine
 - (b) Compare following programmble Logic Devices : PROM and PLA and PAL
 - (c) Draw the state diagram and the state table for a Moore type sequence detector to detect the sequence 110.
 - (d) Explain various semiconductor memories in detail.

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